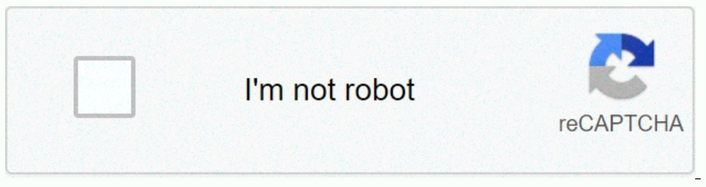

Continue

Phase lock loop ic

Click on the image to enlarge it The LM565 is a general purpose PLL (phase lock loop) IC designed for demodulation, frequency multiplication, and frequency division. The device mainly consists of two components, one is a voltage control unit oscillator and the other is a phase detector. VCO is designed for PD with very linear operation and good carrier suppression. The pin configuration LM565 is a 14-pin device, and the functions of each pin are described below. Pin name function 1 -Vcc negative supply input pin 2 Input phase detector input pin (FM signal input) 3 Input phase detector input pin (FM signal input) 4 VCO output VCO (voltage controlled oscillator) output 5 phase com function VCO input phase detector input pin (VCO output is feedback through this pin) 6 Reference output Internal amplifier reference output 7 VCO control voltage V CO control voltage can be seen at the free running frequency of VCO 9 with this pin 8 timing resistor VCO 10 +Vcc positive power supply 11 NC timing capacitor capacitor for un disconnected free running frequency 12 NC no connection 13 NC no connection 14 NC no connection LM565 Function and characteristics Wide power supply range 0 Linearity of 2% of demodulation output TTL and DTL compatible detector inputs and square wave outputs available at phase zero intersections ± from 1% > C frequency stability of the maximum operating frequency of hold VCO VCO adjustable in the ±60% 200 ppm/° range: 500KHz operating voltage range: ±5V to ±12V Maximum operating voltage: ±12V Operating temperature range: -55ºC to +12 5ºC storage temperature range: -65°C to +150°C Supply current: 12.5mA Maximum power dissipation: 1400mW ICs MAX2880, 74HC The T9046A, 74LV4046A LM565 IC Overview LM565 is essentially used in applications where PLL is required, such as FM demodulation and signal frequency oscillators and powers. The device specifically designed a highly linear VCO for low distortion FM modulation. Cheap devices can be used in applications where cost is taken into account. For circuit-first use of the LM565 IC, consider the internal block diagram of the LM565 PLL chip. To understand, you can further simplify this block diagram to get: An input analog signal can be connected to device pins 2 and 3, but pin 3 is usually grounded and pin 2 is used as the input. The input signal enters the phase detector with VCO feedback, which compares whether both signals are in the same phase (or frequency). If they are in phase (or frequency), the PD provides a zero voltage output, and if phase (or frequency) is present, the PD provides a positive output voltage. The output voltage of this PD is given to the amplifier to amplify the voltage signal, and the amplified voltage is given to the VCO that produces the waveform with the frequency.for the magnitude of a given input voltage. Where the VCO is a free-running mode generation signal who is frequency determined by capacitors and resistors connected to pins 8 and 9. When a signal is given at the input, the frequencies of both the input signal and the VCO output are compared. And if they do not match, the PD is amplified to provide the voltage supplied to the VCO. The VCO increases or decreases the signal frequency depending on the supply voltage of the amplifier. When the adjustment is complete, both the input signal frequency and the VCO frequency match. This is how a phase lock loop works, and the VCO output signal frequency always trys to keep up with the input signal frequency. Application FSK and FM demodulation data and tape synchronization modem frequency synthesizer tone decoding frequency multiplication and division SCA demodulator telemetry receiver signal reproduction coherent demodulator 2D model demodulator 2D model measurements are PLL redirection in inches and millimeters. For other uses, see PLL (Avoid ambiguity). The simplest analog phase lock loop phase lock loop or phase lock loop (PLL) is a control system that generates an output signal with a phase associated with the phase of the input signal. There are several different types. The simplest is an electronic circuit consisting of a variable frequency oscillator and a phase detector in a feedback loop. The oscillator generates a periodic signal, and the phase detector compares it to the phase of the input periodic signal, adjusting the oscillator to keep the phases consistent. Keeping the I/O phase in the lock step also means keeping the I/O frequency the same. Therefore, in addition to signal synchronization, phase-locked loops track input frequencies or generate frequencies that are multiples of the input frequency. These properties are used to synchronize, demodulation, and frequency synthesis of your computer's clock. Phase lock loops are widely used in wireless, communications, computers and other electronic applications. It can be used to demodule signals, recover signals from noisy communication channels, generate stable frequencies at multiples of input frequencies (frequency synthesis), or accurately deliver timing clock pulses in digital logic circuits such as microprocessors. This technology is widely used in modern electronics, with output frequencies from parts of Hertz to many gigahertz, since a single integrated circuit can provide the building blocks of a complete phase lock loop. Consider a race between two cars, as a practical analogy of a car race parable of a PLL. One represents the input frequency and the other represents the output voltage controlled oscillator (VCO) frequency of the PLL. Each lap corresponds perfectlyThe number of laps per hour (speed) corresponds to the frequency. The separation (distance) of the car corresponds to the phase difference between the two vibration signals. During most of the race, each car is free to pass through the other alone and wrap the other. This is similar to an unlocked PLL. However, in the event of an accident, a yellow caution flag will be raised. This means that neither race car is allowed to overtake and pass other cars. The two race cars represent the I/O frequency of the PLL in a locked state. Each driver measures the phase difference (part of the distance around the lap) between himself and the other race cars. If the back-backed driver is too far away, they increase the speed to close the gap. If they are too close to other cars, the driver slows down. As a result, both race cars circle the track in lockstep with a fixed phase difference (or constant distance) between them. Neither car is allowed to wrap the other car, so the car makes the same number of laps over a period of time. Therefore, the frequencies of the two signals are the same. The phase difference is the time difference because the parable phase of the clock can be proportional to time[a]. The clock is a leader clock with phase lock (time lock) with different degrees of accuracy. Leaving alone, each clock marks the time at a slightly different rate. For example, wall clocks can be as fast as a few seconds per hour compared to NIST reference clocks. Over time, the time difference will be substantial. To keep it in sync with the reference clock, every week, the owner compares the time of the wall clock to a more accurate clock (phase comparison) and resets the clock. If left unattended, the

wall clock continues to emanate from the reference clock in the same seconds per hour. Some clocks have timing adjustments (fast slow control). When the owner compared the wall clock time to the reference time, they noticed that the clock was too fast. As a result, the owner can change the timing adjustment to a little (frequency) so that the clock runs a little slower. When things go well, their watches will be more accurate than before. In a series of weekly adjustments, the concept of the second of the wall clock agrees with the reference time (locked in both frequency and phase within the stability of the wall clock). Early electromechaned versions of phase-locked loops were used in short synchronome clocks in 1921. The spontaneous synchronization of the history-weakly coupled resonist clock was noted as early as 1673 by dutch physicist Christian Huygens. At the turn of the 19th century, Lord Rayleigh observed the synchronization of weakly coupled organ pipes and tuning forks. In 1919, W.H. Eccles and J.H. Vincent had two electron oscillatorsIt was adjusted to vibrate at slightly different frequencies, but would soon vibrate at the same frequency, coupled to a resonant circuit. [3] Automatic synchronization of electronic oscillators was described in 1923 by Edward Victor Appleton. In 1925, Professor David Robertson, the first professor of electrical engineering at the University of Bristol, introduced phase locking to the design of the watch to control the blow of the Bell Great George at the new Virus Memorial. Robertson's watch incorporated an electromechanic device that could change the vibration rate of the reiko, deriving the correction signal from a circuit that compares to the reiko phase of the incoming telegraph pulse from the Greenwich Observatory at 10.00 GMT each morning. Other than the equivalent of all elements of a modern electronic PLL, Robertson's system was notable in that its phase detector was a relay logic implementation of a phase/frequency detector not found in electronic circuits until the 1970s. Robertson's research pre-empted research towards what was named a phase-locked loop in 1932, when British researchers developed an alternative to Edwin Armstrong's superheterodyne receiver, homodyne or direct conversion receiver. In a homodyne or synchronized system, the local oscillator was adjusted to the desired input frequency and the input signal was multiplied. The resulting output signal contained the original modulation information. The aim was to develop an alternative receiver circuit with fewer adjusted circuits than a superheterodyne receiver. Because the local oscillator drifts rapidly at frequencies, an automatic correction signal was applied to the oscillator to maintain the desired signal at the same phase and frequency. The technique was described in the French journal L'Onde Électrique in 1932 in a paper by Henri de Belectrique. [5] [6] In analog TELEVISION receivers, the horizontal and vertical sweep circuits of the phase lock loop are locked to the synchronous pulse of the broadcast signal since at least the late 1930s. When on semiconductor HC4046A introduced a series of monolithic integrated circuits such as ne565 in 1969, the application of the technology adopted a complete phase-locked loop system on the chip in 1969 was multiplied. A few years later, RCA introduced the CD4046 CMOS micropower phase lock loop, which became popular as an integrated circuit. Structural and functional phase lock loop mechanisms can be implemented as analog or digital circuits. Both implementations use the same basic structure. Analog PLL circuits have four basic elements: a phase detector, a low-pass filter, a voltage-controlled oscillator, and a feedback path (which may include a frequency parting device). There are several variations of variation Pll. Some of the terms used are analog phase lock loops (APLL)Linear phase lock loops (LPLL), digital phase lock loops (DPLL), all digital phase lock loops (ADPLL), and software phase lock loops (SPLL). [10] Analog or linear PLL (APLL) phase detectors are analog powers. The loop filter is active or passive. Use a voltage-controlled oscillator (VCO). APLL is called type II if the loop filter has a transfer function with one pole at the origin (see also Egan's guess about the pull-in range of type II APLL). An analog PLL with a digital PLL (DPLL) digital phase detector (XOR, edge trigger JK, phase frequency detector, etc.). The loop may contain a digital divider. Digital PLL (ADPLL) phase detectors, filters and oscillators are all digital. Use a numerical control oscillator (NCO). Software PLL (SPLL) functional blocks are implemented by software, not special hardware. The charge pump PLL (CP-PLL) CP-PLL is a modification of the phase lock loop using a phase frequency detector and a shaped waveform signal. See also Gardner's guesses about CP-PLL. Performance parameters Main article: Phase lock loop range type and order. Frequency range: hold-in range (tracking range), pull-in range (capture range, acquisition range), lock-in range[11]. See also Egan's guesses about Gardner's problems in the lock-in range, the pull-in range of type II APLL. Loop bandwidth: Defines the speed of the control loop. Pass response: To calm time to overshoot and constant accuracy (for things like 50 ppm). Steady-state errors: Similar to the remaining phases and timing errors. Output spectral purity: similar to sidebands generated from specific VCO tuning voltage ripples. Phase noise: Defined by the noise energy in a specific frequency band (such as a 10kHz offset from the carrier). It is heavily dependent on VCO phase noise, PLL bandwidth, etc. Common parameters: Application phase lock loops, such as power consumption, supply voltage range, and output amplitude, are widely used for synchronization purposes. In space communication for coherent demodulation and threshold expansion, bit synchronization, and symbol synchronization. Phase lock loops can also be used to demodule frequency modulated signals. Radio transmitters use PLL to synthesize new frequencies, which are multiples of reference frequencies, with the same stability as the reference frequency. For other applications, if the frequency modulation (FM) :P LL is locked to the FM signal, the VCO tracks the moment frequency of the input signal. A filtered error voltage that controls the VCO and maintains the lock on the input signal demodules the FM output. The VCO transfer characteristics determined the demodulation linearity. Since the VCO used in integrated circuit PLL is high-wire, it is possible to realize a high-wire FM demodulator. Frequency Shift Keying (FSK): Demodulation in Digital Data CommunicationsComputer peripherals are transmitted by carrier frequencies where binary data is off between two preset frequencies. Recovery of small signals lost due to noise (lock-in amplifier for tracking reference frequencies) The microprocessor clock count, which allows internal processor elements to operate faster than external connections, recovers clock timing information from the data stream from the disk drive, and accurately adjusts modems and other tone signals for communication and remote control while maintaining an accurate timing relationship. Dsp of video signals; phase-locked loops are also used to synchronize phases and frequencies to analog video signals for sampling and digitally processed atomic force microscopy in frequency modulation mode to detect changes in cantity resonance frequencies due to tip-to-surface interactions. The receiver generates a clock from approximate frequency criteria and uses a PLL to phase-align transitions in the data stream. This process is called clock recovery. For this scheme to work, the data stream needs to transition frequently enough to correct the drift of the PLL oscillator. Typically, certain line codes, such as 8b/10b encoding, are used to set a hard limit on the maximum time between transitions. If you send a clock in parallel with the data you skew, you can use that clock to sample the data. Because the clock must be received and amplified before driving the flip-flops that sample the data, there is a finite, process, temperature, and voltage-dependent delay between the detected clock edge and the received data window. This delay limits how often data can be sent. One way to eliminate this delay is to remove the pLL from the receiving end so that the clock on each data flip-flop is phase-matched with the receiving clock. These applications frequently use a special form of PLL called a delayed lock loop (DLL). [12] The generation of watches Many electronic systems contain various types of processors that operate in hundreds of megahertz. Typically, the clocks supplied to these processors are obtained from the clock generator's Pll and multiply the low-frequency reference clock (typically 50 MHz or 100 MHz) by the processor's operating frequency. The multiplication factor can be very large when the operating frequency is multiple gigahertz and the reference crystal is tens or hundreds of megahertz. All electronic systems in the spread spectrum emit some unwanted radio frequency energy. Various regulatory bodies (such as the US FCC) have placed limits on emissionsAnd any interference caused by it. Radiated noise generally appears at sharp spectral peaks (usually the operating frequency of the device, and some harmonics). By dispersing energy across much of the spectrum, system designers can use spread-spectrum PLL to reduce interference with high-Q receivers. For example, by changing the operating frequency little by little (about 1%), devices operating at hundreds of megahertz can evenly distribute interference across a spectrum of several megahertz, significantly reducing the amount of noise seen on broadcast FM radio channels with bandwidths of tens of kilohertz. Clock distribution Typically, the reference clock enters the chip and drives a phase-locked loop (PLL) to drive the clock distribution of the system. The distribution of clocks is usually balanced so that the clock arrives at all endpoints at the same time. One of these endpoints is the PLL feedback input. The function of the PLL is to compare the distributed clock to the input reference clock and change the phase and frequency of the output until the reference clock and feedback clock match the phase and frequency. Pll is ubiquitous, adjusting the clock for a few feet of system as well as adjusting the clock with a small part of the individual chip. In some cases, the reference clock is not actually a pure clock, but a data stream with sufficient transitions that the PLL can recover the normal clock from that stream. Sometimes the reference clock is the same frequency as the clock driven through the clock distribution, and the other multiple dispersion clocks may be some rational multiple of reference. The AM detection APLL can be used to synchronously demodule the amplitude modulation (AM) signal. The PLL recovers the carrier phase and frequency of the incoming AM signal. The VCO-recovered phases have 90° different carrier phases, so the phase is shifted to match and supplied to the power. The output of the power includes both the total and the differential frequency signal, and the demodulation output is obtained by low-pass filtering. Because the PLL responds only to carrier frequencies very close to the VCO output, the PLL AM detector provides high selectivity and noise immunity that traditional peak AM demodulators cannot. However, if the AM signal has a modulation depth of 100%, the loop can lose lock. [13] Jitter and noise reduction One of the desirable characteristics of all PlL is that the reference and feedback clock edges are very close. The mean time difference between the phases of the two signals when the PLL achieves a lock is called a static phase offset (also known as steady-state phase error). The distribution between these phases is called tracking jitter. Ideally, the static phase offset should be zero.The tracking jitter should be as low as possible. [Suspicious – Argument] Phase noise is another type of jitter observed in the Pll and is caused by the oscillator itself and the elements used in the oscillator's frequency control circuitry. Some technologies are known to perform better than others in this regard. The best digital PlL is built with emitter-coupled logic (ECL) elements at the expense of high power consumption. If you want to keep the phase noise of your PLL circuitry low, it is best to avoid saturation of logic families such as transistor transistor logic (TTL) and CMOS. [14] Another desirable characteristic of all PlL is that the phase and frequency of the generated clock are not affected by a sudden change in the voltage between the power supply and ground supply line, and a change in the voltage of the board on which the PLL circuit is manufactured. This is called board and feed denoising. The higher the denoising, the better. To further improve the phase noise of the output, an injection lock oscillator can be adopted following the VCO of the PLL. Frequency synthesis Digital radio communication systems (GSM, CDMA, etc.) use PPL to up-convert local oscillators during transmit and down conversion at reception. In most mobile phone phones, this feature is mainly integrated into a single integrated circuit to reduce the cost and size of the phone. However, due to the high performance required for base station terminals, transmit and receive circuits are built with individual components to achieve the required level of performance. GSM local oscing modules are typically built using frequency synthesizer integrated circuits and discrete resynthemer VCAs. The block diagram of the Phase Lock Loop A Phase Detector compares the two input signals and generates an error signal proportional to their phase difference. Error signals are filtered in a low pass and used to drive the VCO that creates the output phase. The output is returned to the system input through an optional divider, generating a negative feedback loop. As the output phase drifts, the error signal increases and the VCO phase drives in the opposite direction, reducing errors. Therefore, the output phase is locked to the phase at other inputs. This input is called a reference. Analog phase lock loops (citation required) are typically constructed with analog phase detectors, low-pass filters, and VCAs in negative feedback configurations. The digital phase lock loop uses a digital phase detector. It may also have a divider in the feedback path or reference path, or both, to make the output signal frequency of the PLL a rational multiple of the reference frequency. Non-integer multiples of the reference frequency can also be created by replacing a simple N-desaling counter in the feedback path.Programable pulse swallowing counter. This technique is usually called a minute N synthesizer or a minute N PLL. The Suspicious – Argument oscillator generates a periodic output signal. First assume that the oscillator is about the same frequency as the reference signal. When the phase from the oscillator is delayed to the reference phase, the phase detector changes the oscillator's control voltage to increase speed. Similarly, if the phase creeps ahead of the reference, the phase detector changes the control voltage to slow down the oscillator. Since the first oscillator may be far from the reference frequency, a practical phase detector may respond to frequency differences and increase the lock-in range of the allowable input. Depending on the application, either the output of the control oscillator or the control signal to the oscillator provides useful output for the PLL system. [Citation required] Element phase detector main part: Phase detector A phase detector (PD) generates a voltage representing the phase difference between the two signals. In the PLL, the two inputs of the phase detector are reference input and feedback from the VCO. The PD output voltage is used to control the VCO so that the phase difference between the two inputs remains constant and becomes a negative feedback system. [15] Different types of phase detectors have different performance characteristics. For example, frequency mixers produce harmonics that add complexity in applications where the spectral purity of the VCO signal is critical. The resulting (spurious) sideband, also known as a reference spurious, can dominate filter requirements, significantly below the capture range, or increase lock time beyond the requirements. In these applications, more complex digital phase detectors are used less rigorously than reference spar components on their outputs. At the time of locking, the steady phase difference at the input using this type of phase detector is close to 90 degrees. Citation required In PLL applications, you often need to know when a loop is off lock. More complex digital phase frequency detectors usually have outputs that allow for a reliable display of locked state conditions. XOR gates are often used in digital PlL as effective yet simple phase detectors. It can also be used with analogue sensations with minor changes to the circuit. Blocks called filter PLL loop filters (typically low-pass filters) typically have two different features. The main function is to determine the loop dynamics, also known as stability. This is how the loop responds to disturbances, such as changes in the reference frequency, changes in feedback segment lines, and startup behavior. A common consideration is the extent to which the loop can achieve a lock.Range, lock range or capture range, how fast the loop achieves locking (lock time, lock-up time or cetling time) and attenuation behavior. Depending on your application, you may need one or more simple ratios (gain or attenuation), integrals (low-pass filters), and/or derivatives (high-pass filters). The loop parameters that are often examined in this case are the gain margin and phase margin of the loop. Common concepts of control theory, including PID controllers, are used to design this function. The second common consideration is to limit the amount of reference frequency energy (ripple) that occurs at the phase detector output applied to the VCO control input. This frequency regulates the VCO and produces an FM sideband commonly referred to as a reference spris. The design of this block can be governed by any of these considerations, or it can be a complex process juggling two interactions. A common trade-off is that increasing bandwidth typically slows down and essing time increases if it is attenuated too much to reduce stability or improve stability. Phase noise is often also affected. Oscillator Article: The electron oscillator whole-level lock loop employs an oscillator element with the ability to fluctuate frequencies. This could be an analog VCO driven by an analog circuit in the case of an APLL or digitally driven using a digital-to-analog converter as is the case with some DPLL designs. Pure digital oscillators, such as numerically controlled oscillators, are used in AdPL. An example (according to 4) used for the feedback path [citation required] feedback path and any split line PLL PlLs may include a divider between the oscillator and the feedback input to the phase detector that generates a frequency synthesizer. Programmable dividers are particularly useful in radio transmitter applications because they can generate a large number of transmit frequencies from a single stable, accurate, but expensive crystal-controlled reference oscillator. Some Plls also include a break between the reference clock and the reference input to the phase detector. If the feedback path separator is divided by N {\display style N}, and the reference input split is divided by M {\display style M}, the PLL multiplies the reference frequency by N/M {\displaystyle N/M}. Giving the PLL a lower frequency may seem simpler, but in some cases the reference frequency is constrained by other problems, and reference splitting can be useful. Frequency multiplication can also be achieved by locking the VCO output to the Nth harmonic of the reference signal. Instead of a simple phase detector, the design uses a harmonic mixer (sampling mixer). Harmonic mixers turn reference signals into harmonic-rich impulse trains. [b] VCO output is coarsely adjustedto one of those harmonics. As a result, the desired harmonic mixer output (representing the difference between the N harmonic and the VCO output) fits within the passband of the loop filter. It should also be noted that feedback is not limited to frequency dividers. This element can use other elements such as frequency factors and mixers. This power should make the VCO output a sub-multiple of the reference frequency (not more than one). The mixer can convert the VCO frequency at a fixed offset. It may also be a combination of these. An example of a divider following a mixer. This allows the divider to operate at much lower frequencies than the VCO without compromising loop gain. Equations governing a phase lock loop having an analog number as a modeling time domain model phase detector and linear filter of the APLL can be derived as follows. The input to the phase detector is f 1 (θ 1 (t)) {\display style f_{1}(\theta _{1}(t)}, and the output of the VCO is f 2 (θ 2 (t)) { \ display style f_{2} Phase θ1 (t) {\display style \θ_{1}(t)} and θ 2 (t) {\display style \θ _{2}(t)} with (\theta _{2}(t)}. Functions f 1 (θ) {\display style f_{1} (\theta)} and f 2 (θ) {\display style f_{2}(\theta)} describe the waveform of the signal. Next, the output of the phase detector φ (t) {\displaystyle \varphi (t)} is φ (t) = f 1 (θ 1 (t)) f 2 (θ 2) f 2 (t) {\ display style \varphi (t)=f_{1}(\theta_{1} {2}(t)) f_{2}(\theta_{2}(t)}) style g(t)} θ 2 (t) = ω 2 (ω 2) = ω 2 (t) = g v g (t) {\display style {\dot {\theta}\{2}(t)=\ω _{2}(=\ω)=\ω _{{text{free}+g_{v}g(t)g_, g_{v}g(t),}VCO sensitivity is shown. ω-free {\display style \ω _{\text{free}} is the free running frequency of the VCO. Loop filters can be written with linear differential equations x X = A x + b φ (t), g (t) = c ∗ x , x (0) = x 0 , {\display style {start array}{{rcl}{\dot {x}&ax+b\varphi (t),. \\g(t)=c^{}x,\end{array}\quad x(0)=x_{0},} φ (t) {\display style \varphi (t)} is the input of the filter, and g (t) {\display style g(t)} is the output of the filter. {\Display style A} is n {\displaystyle n} - n {\displaystyle n} matrix, x ∈ C n, b ∈ R n, c ∈ C n, {\display style x\in \mathbb {C} ^{n}, \quad b\in \mathbb {R}x 0∈ C {\displaystyle x_{0}\in \mathbb {C} ^{n}} Represents the initial state of a filter. The symbol of the star is conjugate transconjugate trans junts. Therefore, the following systems describe PLL x = A x + b f 1 (θ 1 (t) f 2 (θ 2 (t) , θ 2 = ω free + g v (c ∗ x) x (0) = x 0 , θ 2). {\display style {\begin{array}{rcl}{\dot {x}}}&Ax+bf_{1}(\theta _{1}(t)) f_{2}(\theta)\{\theta }} _{2}=\ω _{\text{free}}+g_{v}(c^{*x)\end{array}\quad x(0)=x_{0},\quad\teta_{2}(0)=\teta_{0}.} θ 0 {\Display style \θ _{0}} is the initial phase shift. Consider the input of the phase domain model PLL f1 (θ 1 (t) for the APLL (\\ display style f_{1} (\θ _{1}(t)}) and VCO output f2 (θ 2 (t)) {\display style f_{2} (\theta _{2}(t)). Then any partially π {\displaystyle 2\pi } - periodic function f 1 (θ) {\display style f_{1}(\theta)} and f 2 (θ) {\display style f_{2} (\theta)} has a function φ (θ) {{ filter x ○ = A x + b φ (θ 1 (t) - θ 2 (t), G (t) = output G of c ∗ x x (t) { \displaystyle G(t)}, x (0) = x 0 , {\display style {\start{array}{rcl}{\dot {x}&axe+b\barify (\t ta_{1})-\teta_{2}(t)), \G(t)==&c^}} x,\end{array}\quad x(0)=x_{0},} The phase domain discount equal (difference G (t) - g (t) {\ display style G(t)-g(t)} is small for the output of the filter in the time domain model. [16] [17] The φ here (θ) {\display style \varphi (\theta)} is a phase detector characteristic. θ Δ (t) {\ display style \θ _{\delta } (t)} Phase difference θ Δ = θ 1 (t) - θ 2 (t). {\Display style \teta _{\delta }=\teta _{1}(t)-\teta _{2}(t)}Next, the following dynamic systems describe PLL operation x○ = A x + b φ (θ Δ), θΔ = ω Δ - g v (c∗x). x (0) = x 0 , θ Δ (0) = θ 1 (0) - θ 2 (0) 。 {\display style {\begin{array}{rcl}{\dot {}&&Ax+b\varphi (\theta _{\delta}),\dot {\theta }\\delta\%\mega_\delta }-- g_{v}(c^{*x).\end{Array}\quad x(0)=x_{0},\Quad\Teta_{\Delta}(0)=\Teta_{1}(0)-\ Teta_{2}(0)}where ω Δ = ω 1 - ω free {\display style \ω _{\delta =\ω _{1}-\ω _{\text{free}} } ;ω 1 {\display style \ω _{1}} is the frequency of the reference oscillator (assuming the ω-free {\display style \ω _{\text{free}} is constant). Example: Sign-idal signal f 1 (θ 1 (t) = A 1 sin (θ 1 (t) , f 2 (θ 2 (t)) = A 2 cos (θ 2 (t))) { \ display style f_{1} (\theta _{1} (t)=A_{1}\sin(\theta _{1}(t)), \quad f_{2}(\theta _{2}(t)=A_{2}\cos(\theta _{2}(t)) and a simple one-pole RC circuit as a filter. The time domain model is x= - 1 R C x + 1 R C 1 A 2 {2} (θ 1 (t) cos (θ 2 (t) , θ 2 = ω free + g v (c ∗ {1} x) {\Display style {\\Take display style Start {\dot {x}}{{dot {x}={frac {1}{RC}}x+{{1}{{1}{RC}}A_{1}A_{2}\sin(\\ theta _{1}(t)\cos(\theta _{2}(t)),\\[6pt]{\theta}\{2}=\Omega _{\Text{Free}+g_{v}(c^{}x)\End} What is the PD characteristic of this signal? Equal [18] φ (θ 1 - θ 2) = A 1 A 2 2 Sin (θ 1 - θ 2) {\Display style \varphi (\θ _{1}-\θ _{2})={\ frac_{1}-\theta _{2}}} Therefore, the phase domain model is in the form of x = - 1 R C x + 1 R C A 1 A 2 2 sin (δ), θΔ = ω Δ - g (c ∗ x). {\Display Style {\Start{Alignment}{x}{dot {x}}-{frac {1}{RC}}x+{{frac {1}{RC}}{frac {A_{1}A_{2}}{2}}\sin() \theta)\theta _{\delta }, \[6pt]{\dot{\θ}\\delta}{\delta}=\mega{\delta}-g_{v}(c^{*}x)\end{alignment} The equation for this equation is mathematical reiko x = θ 2 - ω 2 g v c ∗ = ω 1 - θ Δ - ω 2 g v c ∗ ∗, x θ = θ 2 g v c ∗ , θ 1 = ω 1 t t + Ω 1 t ○ θ ○ 2 = ω 1 - θ 、 1 g v c ∗ θ δ - 1 g v c ∗ R C θ Δ Δ — A 1 A 2 2 R C sin θ Δ = ω 2 - ω 1 g v c ∗ R C . {\Display style {\Start{Align}x&==\frac {{\dot {\theta}}{2}-\ω _{2}}{g_{v}c^}{frac{\ω_{1}-\dot{\the t }}\\Delta }-\Omega _{2}}{g_{v}c^{}\6pt]{\dot{x}}\ddot {\theta}{2} g_}{{2}}{v }c {},\ [6pt]\θ_{1}==\Omega_{1}t+\Psi\Δ{=\Teta_{1}-\Teta_{2}\18 [6pt]{\dot {\theta }\{{ \Delta}&={\dot{\theta}{1}-{\dot{\theta}{2}=\Omega_{1}-{\dot{\teta}{2}{1} g_{{v}c^{{\ddot{{{ theta}}{v}c^g_ c^}RC}}{{1}{{1}{v}c^{RC}{dot{\theta}{\{\fra A_{1}A_{2}c{{2RC}}\s in \theta _{\Delta}{frac {\ω _{2}-\omega _{1}}{g_{v}c^{}RC}\{end aligned}\{end aligned}}} Linearized phase domain model phase lock loops can also be analyzed as control systems by applying Laplus transformations. The loop response is θ o θ i = K p K v F (s) + K p K V F (s) + K p K V F (s) {\frac {\theta _{o}{{ You can write as \theta _{i}}{θ_{i}}{K_{{θ{p}K_{v}F(s){s+K_{p}. }K_{v}F(s)}} Where θ o {\displaystyle \theta _{o} is the output phase K_ radians. v {\displaystyle K_{v}} has a VCO gain (voltsecond F (s) {\display style F(s)) is a loop filter transfer function (nondimensional) loop characteristics that can be controlled by inserting different types of loop filters. The simplest filter is a one-pole RC circuit. In this case, the loop transfer function is F (s) = 1 1 + s R C {\display style F(s)={\frac {1}{1+sRC} loop response is as follows: \theta _{i}={frac{K_{p}K_{v}{RC}{2}{frac{K_{K_ p}{}{}RC}This is a classic harmonic oscillator format. The denominator has a secondary system association: s 2 + 2 s ζ ω n + ω n 2 {\display style s^{2}+2s\zeta \omega _{n {2}}ζ {display style \zeta} is the damping factor, and ω n {\display style \ω _n}} is the natural frequency of the loop. For a 1-pole RC filter, ω n = K p K v R C\ω _{n}{\sqrt{{K_ K_{RC} ζ = 1 2 K p K V R C {\display style \zeta ={\frac {1}{2{sqrt{K_{p}K_{v}RC} The natural frequency of the loop is a measure of the loop response time. The attenuation factor is a measure of overshoot and ringing. Ideally, the natural frequency should be high and the attenuation factor should be close to 0.707 (critical damping). Single-pole filters do not allow you to control the loop frequency and attenuation factor separately. For critical damping, R C = 1 2 K P K v {frac {1}{2K_{p}K_{v} ω c = k v 2 {\display style \ω _c}=K_{p}K_{v}\}{\sqrt {2}}A slightly more effective filter, and a lag lead filter contains 1 pole and zero. This can be realized with two resistors and one capacitor. The transfer function for this filter is F (s) = 1 + s C 2 1 + s C (R 1 + R 2) {\display style F(s)={\frac {1+sCR_{2}}{1+sC(R_{1}+R_{2})}}This filter has two time constants. τ 1 = C (R 1 + R 2) {\display style \t _{1}=C(R_{1}+R_{2}}} τ 2 = C R 2 {\display style \tau _{2}=CR_{2}} In addition, the following natural frequencies and attenuation factors ω n = K p K v ντ 1 {\display style \ω _{n}={{\sqrt {\frac {K_{p}K_{v}{\tau _{1}} ζ = 1 2 ω n τ 1 + ω n 2 2 {\display style \zeta ={\frac {1}{2\ω _{n}\tau _{1}}}{}\.\frac {\omega _{n}\t au _{2}}{2}}Loop filter component has a given natural frequency and attenuation factor of τ 1 = K p K v ω n 2 {\display style \{1}={frac {K_{p}K_{v}{2}} 2 = 2 ζω n - 1 K p K v {\display style \tau _{2}={\frac {2\zeta}{\ω _n}}}~{K_ {1}{p}K_{v} Real-world loop filter designs can be more complex. Implementing a digital phase lock loop in software (see D-Banergy below) A digital phase lock loop can be implemented in hardware using an integrated circuit such as cmos 4046. However, with the speed of the microcontroller, it may make sense to implement a phase lock loop in the software for applications that do not need to lock signals above the MHz range ,such as precise control of motor speed. The software implementation has several advantages, including easy customization of the feedback loop, such as multiplying the tracked signal with the output oscillator and changing the division ratio. In addition, the implementation of the software will help you understand and experiment. As an example of a phase lock loop implemented using a phase frequency detector, this type of phase detector is introduced in MATLAB because it is robust and easy to implement. % This example is written with matlab % initialization variable vcofreq = zero (1, number). ervec = zero (1, number). % Track references, signals, and last state,Signal qsig = 0;qref = 0;lref = 0;lsig = 0;Relsig = 0;phs = 0;freq = 0;% Loop filter constant (proportional and differential) % Currently, two powers to facilitate multiplication by shift prop = 1 / 128. Derivation = 64;for it = 1:numiterations % 16-bit counter phs = mod(phs + 2^16), 2^16 to simulate a local oscillator. Ref = phs < 32768;% sig = tracksig(it) Gets the next digital value (0 or 1) of the signal. Implement the % phase frequency detector rst = ~ (qsig and qref). % qsig = (qsig |) with high both signal and reference sig &~lsig)) and rst;% trigger signal flip-flops and leading edges of signal qref = (qref |(reference and ~lref)) and rst;reference reference = ref triggers a trigger reference flip-flop on the leading edge. lsig = sig;% For the next iteration (edge detection), store these values. Calculate the % error signal (whether or not the frequency increases or decreases) % The error signal implements a polar zero filter with proportional and differential inputs to either flip-flop signal % frequency filtered_ersig = ersig + (Elsig - lersig) * derivatives. Proportional output Larsig = Elsig% keep error signal. % Error signal freq = freq - 2^16 * filtered_ersig * prop to integrate VCO frequencies. % frequency is tracked as fixed point bi-minute % % current VCO frequency vcofreq(1, it) = freq / 2^16. % Save the error signal to indicate whether the signal or reference is a higher frequency ervec(1,it)=ersig. end In this example, the array track sig is believed to contain the reference signal to be tracked. The oscillator is implemented by the counter, and the top bit of the counter indicates the oscillator's on/off status. This code simulates two D-type flip-flops that make up a phase frequency comparator. If the edge of the reference or signal is positive, the corresponding flip-flop switches high. If both the reference and signal are high, both flip-flops are reset. Which flip-flop is higher determines whether the reference or signal is leading the other at that moment. The error signal is the difference between these two flip-flop values. The extreme zero filter is implemented by adding an error signal and its derival function to the filtered error signal. It is integrated to find oscillator frequencies. In practice, you may want to insert other operations into the feedback for this phase lock loop. For example, if a phase lock loop implements a frequency number, the oscillator signal can be divided by frequency before comparing it to the reference signal. Frequency Lock Loop Charge Pump Phase Lock Loop Carrier Recovery Circle Map - See a simple mathematical model of a phase lock loop showing both mode locking and chaotic behavior. Kovas Loop Delay Lock Loop (DLL)Conversion Receiver Direct Digital Synthesizer Kalman Filter PLL Multi-Bit Short Synchronome Clock - Slave Reiko Phase Lockmaster (ca 1921) Note ^ If the frequency is constant and the initial position is zero, the phase of the sinusid is proportional to time. ^ Typically, the reference positive wave drives the step recovery diode circuit to create this impulse train. The resulting impulse train drives the sample gate. See ^ Christian Huygens, Hologium Osiratrium .. (Paris, France: F. Mughe, 1673), pages 18-19. From page 18: .. Ildok Asidit Memul Dignam 、.. Brevi Tempore Reducelet (... It's worth mentioning, because it interrupts as well as two clocks built in this form, really crossbeams are assigned two 3D points [i.e., two reiko clocks suspended from the same wooden beam]. The movement of the reiko is clearly audible together because the two clocks do not travel even at small distances, so the move of the reiko shares the reverse swing between the two [clocks]. English translation provided by Ian Bruce's translation of hologium osiratrium., page 16-17.^ See: Lord Rayleigh, Theory of Sound (London, UK: Macmillan, 1896), vol. 2. Synchronization of organ pipes at the opposite stage is mentioned on §322c, page 221-222. Lord Rayleigh (1907) Acoustic Notes — VII Philosophy Magazine, Series 6, 13:316-333. See Tuning forks with a slight reciprocal effect. ^ See: Vincent (1919) In several experiments in which two adjacent vibration circuits affect the resynation circuit, Proceedings of the Physical Society of London, 32,pt, 84-91.W. H. Eccles and J. H. Vincent, British Patent Specification, 163 : 462 (February 17, 1920).^ E. V. Appleton (1923) Automatic Synchronization of Trio de oscillators, Cambridge Proceedings of philosophy, 21 (Part 3): 231-248. Available online in the Internet Archive. ^ Henri de Berejidze, La Reception Synchrone, Rondo Electric (later: Revue de Lexite et de Ronetic), vol.11, 230-240 pages (June 1932). ^ Reference: French Patent No. 635,451 (Filed on October 6, 1931, Published September 29, 1932). U.S. Patent Synchronous System No. 1,990,428 (filed on September 29, 1932, issued on February 5, 1935). ^ NOTES FOR UNIVERSITY OF LPH COURSE EXPLAINING ILL AND EARLY HISTORY, IC PLL Tutorial included 2009-02-24 Archive on Wayback Machine ^ National Television Systems Committee Video Display Signal IO.Sxlist.com. Acquired 2010-10-14. ^ A.B. Greveen, H. R. Kamenincind, Phase Lock as a New Approach for Tuned Integrated Circuits, ISSCC Digest of Technical Papers, pp.February 1969 ^ Roland E. Best (2007). Phase Lock Loop: Design, Simulation and Application (6th) McGauhill. ISBN 978-0-07-149375-8.^ Leonov, G. A. Kuznetsov, N.V. Yurdashev, M.V. Jurdashev, R.V. (2015). Hold-in, pull-in, and lock-in ranges in PLL circuits: strict mathematical definitions and limitations of classical theory. IEEE transactions in circuits and system I: available paper. Ieee. 62 (10): 2454–2464.arXiv:1505.04262.Doi:10.1109/TCSI.2015.2476295. S2CID 12292968.^ M Horowitz;C. Yang; S. Sidi Lopros (1998-01-01). High-speed electrical signals: overview and limitations (PDF). IEEE Micro. Archived from 2006-02-21 original (PDF). ^ Dixon, Robert (1998), Radio Receiver Design, CRC Press, p. 215, ISBN 0824701615 ^ BasaUbijoy Purkayasta; Kandalpa Kumar Salma (2015).Digital phase lock loop-based signal and symbol recovery system for wireless channels. India: Springer (India) Co., Ltd. (Springer Cinece + Part of Business Media). p. 5.ISBN 978-81-322-2040-4.^ Basab Bijoy Purkayasta; Kandalpa Kumar Salma (2015).Digital phase lock loop-based signal and symbol recovery system for wireless channels. India: Springer (India) Co., Ltd. (Springer Cinece + Part of Business Media). p. 94.ISBN 978-81-322-2040-4.^ G. A. Leonov, N. V. Kuznetsov, M. V. Yurdashev, R. V. Yurdashev; Kuznetsov; Yurdashev; Yurdashev (2012). Analytical Methods for Calculating Phase Detector Characteristics (PDF) IEEE Transactions on Circuits and Systems II: Express Briefs 59 (10): 633–637.Doi: 10.1109/TCSI.2012.2213362.S2CID 24 05056.CS1 Maint: Multiple Names: Author List (link) ^N.V. Kuznetsov, G.A. Leonov, M.V. Yurdashev, R.V. Yurdashev; Leonov; YurdaShev; YurdaShev (2011). Analytical methods for calculating phase detector characteristics and PLL design. ISSCS 2011 – International Symposium on Signals, Circuits and Systems, Minutes: 7-10.Doi:10.1109/ISSCS.2011.5978639.ISBN 978-1-61284-944-1 7.S2CID 30208667.CS1 maint: Multiple Names: Author List (link) ^A.J. Viterbi, Principles of Coherent Communication, Read More On McGow Hill, New York, 1966 Wikimedia Commons has media related to phase lock loops. Banerjee, Dean (2006), PLL Performance, Simulation and Design Handbook (4th), National Semiconductor, was archived from the original on 2012-09-02 and obtained 2012-12-04. Best, R.E. (2003), Phase Lock Loop: Design, Simulation and Application, McGrow Hill, ISBN 0-07-141201-8 Berserise, Henri (June 1932), La Reception Synkune , L'Onde Electcique, 11: 230-240 Dolph, Richard C. (1993), Handbook of Electrical Engineering, Boca Raton: CRC, Bi9.19.19. D, ISBN 0-8493-0185-8 Egan, William F. (1998), Foundations of Phase Rock, John Wiley & Sons. (Provides convenient Matlab scripts for simulation) Egan, William F. (2000), phase-locked frequency synthesis (Part 2), John Wiley, andGardner, Floyd M. (provided a convenient Matlab script for simulation) (2005), Phase Rock Technique (3rd ed.), Wiley Interscience, ISBN 978-0-471-43063-6 Clapper, J.; Frankle, J.T. (1972), Phase Lock and Frequency Feedback System, Academic Press. (FM Demoderge) Kundert, Ken (August 2006), Predicting Phase Noise and Jitter in PLL Bass Frequency Synthesizers (PDF), Designers Guide Consulting, Liu, Meisei (February 21, 2006), 1.5-V 2.4-GHz CMOS PLL, Wireless Net Design Line, July 1, 2000 Articles about designing standard PLL ICs for Bluetooth applications. Worrever, Dan H. (1991), Phase Lock Loop Circuit Design, Prentice Hall, ISBN 0-13-662743-9 External Link Phase Lock Loop Primer - Embedded Video Excel includes an unusual animated PLL model and a tutorial to code such models.